REMARKS

Claims 1-20 are pending in the present application.

Claim Rejections-35 U.S.C. 103

Claims 1-3, 5-7 and 9-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Weber et al. reference (U.S. Patent No. 6,242,789) in view of Japanese Patent Publication No. 4-348517 and the Houston reference (U.S. Patent Application Publication No. 2002/0086465). This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 1 includes in combination a dielectric sidewall structure "formed on the side face of the through hole so that the dielectric sidewall structure gradually narrows the through hole"; and a fuse "formed of a conductive material that buries the narrowed through hole, said fuse having a lower end connected to the first conductive layer and an upper end connected to the second conductive layer". Applicant respectfully submits that the semiconductor device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has primarily relied upon the Weber et al. reference. The Examiner has however acknowledged that the sidewalls within fuse hole 102 as illustrated in Fig. 14 of the Weber et al. reference are not gradually narrowed and are not a dielectric sidewall structure. In order to overcome these acknowledged

deficiencies of the Weber et al. reference, the Examiner has relied upon Japanese Patent Publication No. 4-348517 as disclosing a contact hole with a polycrystalline semiconductor sidewall that narrows the hole towards the base of the hole, as illustrated in Figs. 7 and 12. The Examiner has further relied upon the Houston reference as disclosing in Fig. 1b a sub-lithographic opening for a back contact or back gate, wherein the sidewall spacers 108 that gradually narrow the hole/opening 106 are an oxide dielectric. The Examiner has alleged that it would have been obvious to include the required hole narrowing in the required insulating/dielectric sidewall spacers in the Weber et al. reference in view of the secondarily relied upon references, "in order to have a semiconductor device with increased performance". Applicant respectfully disagrees for the following reasons.

A purpose of the present invention as described on page 2, lines 15-17 of this application is to reduce a cross-sectional area of a fuse. As described in the last paragraph on page 1 of the present application, a fuse is blown by Joule heat from a current that flows through the fuse itself. The Joule heat rises as the cross-sectional area of the fuse becomes small. The present invention uses a dielectric sidewall structure in order to narrow a through hole of the fuse, so as to reduce cross-sectional area of the fuse and to thus aid in fuse design and reduce overall size of semiconductor devices.

As described beginning in column 6, line 14 of the Weber et al. reference with respect to Fig. 14, fuse hole 102 includes a CVD aluminum wetting layer 114 on a liner

material layer 104 such as stacked implanted titanium and/or a CVD TiN. Accordingly, fuse hole 102 in Fig. 14 of the Weber et al. reference includes first and second conductive layers, and consequently the cross-sectional area of the fuse is the same as the cross-sectional area of the contact hole itself. In other words, the Weber et al. reference does not disclose or suggest the concept of narrowing cross-sectional area of a fuse by lining the sidewalls of a fuse hole with a dielectric material.

As emphasized on pages 8-9 of the Amendment dated May 26, 2005, Japanese Patent Publication No. 4-348517 discloses a conductive sidewall in a contact hole. However, Japanese Patent Publication No. 4-348517 as relied upon by the Examiner does not specifically describe a fuse or a fuse hole. Also, the sidewall within the contact hole in Japanese Patent Publication No. 4-348517 is conductive. Japanese Patent Publication No. 4-348517 therefore does not disclose or suggest the concept of reducing a cross-sectional area of a fuse by lining the sidewalls of a fuse hole with a dielectric material.

The Houston reference as relied upon by the Examiner discloses a low resistance buried back contact for SOI devices as illustrated in Fig. 1b, wherein oxide sidewalls 108 are deposited within trench 106. However, as acknowledged by the Examiner and as noted above, the Houston reference is concerned with buried back contacts for SOI devices, not with fuses. The Houston reference does not disclose a fuse, or a fuse hole. The Houston reference as relied upon by the Examiner does not disclose or suggest the concept of reducing a cross-sectional area of a fuse by lining

the sidewalls of a fuse hole with a dielectric material. Accordingly, the prior art as relied upon by the Examiner taken singularly or together does not disclose or suggest the features of claim 1.

Applicant further respectfully submits that the Examiner has not established sufficient motivation to modify the fuse structure of the Weber et al. reference in view of the secondarily relied upon references. One of ordinary skill, looking to improve a fuse structure, would have no motivation to consider Japanese Patent Publication No. 4-348517 which discloses narrowing contact holes using polycrystalline semiconductor sidewalls, or the Houston reference which discloses forming sidewalls within low resistance buried back contacts for SOI devices. One of ordinary skill would not consider these secondary references in an effort to modify the fuse device of the Weber et al. reference to have "increased performance", as suggested by the Examiner. In absence of specifically established motivation, this rejection would appear to be based merely upon impermissible hindsight. Applicant therefore respectfully submits that the semiconductor device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 1-3 and 5-7 is improper for at least these reasons.

The semiconductor device of claim 9 includes in combination a dielectric sidewall structure "formed on a side surface of the through hole so that the dielectric sidewall structure gradually narrows the through hole". The semiconductor device of claim 16 includes in combination a dielectric sidewall structure "formed in the through

hole so that the through hole is gradually narrowed by the dielectric sidewall structure to expose the first conductive film". Applicant respectfully submits that the semiconductor devices of respective claims 9 and 16 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 9-20 is improper for at least somewhat similar reasons as set forth above with respect to claim 1.

With further regard to this rejection, only the Houston reference as noted above discloses a dielectric material. However, Fig. 1b of the Houston reference as relied upon by the Examiner merely discloses a single layer sidewall 108. The prior art as relied upon by the Examiner therefore does not disclose dielectric sidewall structures within a fuse hole as including first and second layers. Applicant therefore respectfully submits that claims 3, 11 and 18 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, for at least these additional reasons.

Claim 15 features that the first sidewall film is formed of silicon nitride and that the second sidewall film is formed of silicon oxide. However, Fig. 1b of the Houston reference as relied upon by the Examiner merely describes that sidewall 108 is made of oxide. The prior art as relied upon by the Examiner therefore does not disclose or suggest a dielectric sidewall structure including first and second sidewall films within a fuse hole, wherein the first sidewall film is silicon nitride and the second sidewall film is silicon oxide. Accordingly, Applicant respectfully submits that claim 15 would not have

been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, for at least these additional reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 4 and 8 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicant however respectfully submits that claims 4 and 8 should be considered allowable by virtue of dependency upon claim 1 for the reasons as set forth above, and that amendment of claims 4 and 8 is thus unnecessary.

Applicant respectfully notes that claim 12, as dependent upon claim 9, features that "a thickness of the dielectric sidewall structure is smallest at the semiconductor substrate and becomes gradually larger away from the semiconductor substrate". Since the features of claim 12 are somewhat similar to the features of claim 4, Applicant respectfully submits that claim 12 should be also include allowable subject matter for at least somewhat similar reasons as claim 4. **The Examiner is respectfully requested to clarify the status of claim 12, and the reasons therefor.**

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the

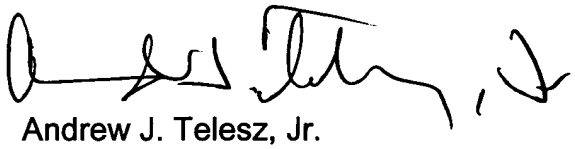
corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740